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USB Superspeed Equalizer Design Guidelines (2011-06-10)
USB 30 SuperSpeed Equalizer Design Guidelines 6 Figure 7 Compliance channel frequency responses for host and device designs Figure 8 Frequency response for an example device design plus compliance channel (a) 10” Host PCB (a) 1” Host PCB Figure 9 Frequency response for example host designs plus compliance channel

cyu - Digi-Key
SuperSpeed Explorer Kit The CYUSB3ACC-007 CPLD Accessory Board is designed to work with the GPIF II of the EZ-USB® FX3™ SuperSpeed Explorer Kit (CYUSB3KIT-003) It is meant to be used for the examples mentioned in the book SuperSpeed Device Design By Example, by John Hyde

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Embedded USB Design By Example, at our behest for those of us known semiconductor supplier in the USB “legacy” device field Our FT232, FT245

and Hi speed dual and quad device series of USB peripheral devices offer a seamless route for easy USB interfacing through proven, well understood serial and parallel interfaces

Getting Started with EZ-USB® FX3™

Cypress provides a wealth of data at wwwcypresscom to help you to select the right FX3 device for your design, and to help you to quickly and effectively integrate the device into your design For a comprehensive list of resources, see SuperSpeed Device Design by Example by John Hyde

AN-6103 - PCB Routing Methodology for SuperSpeed USB 3.1 ...

for SuperSpeed USB 31 Switch Family from ON Semiconductor challenges due to the high speed nature of the interface High Speed USB20 presented enough of a system design challenge for tiny mobile device OEM’s trying to pass USB eye compliance A 10X or even 20X increase in data rates Strips 2B2A Example For SuperSpeed USB the

SuperSpeed USB Design Guidelines

SuperSpeed USB Design Guidelines Howard Heck Pi i lE iPrincipal Engineer Intel Corporation Host Design Example: Mobile Type 3 PCB GuidelinesMobile Type 3 PCB Guidelines Host PCB • 8 layer 85Ωstack-up 2vias •Device Design •Silicon Considerations

Managing Connector and Cable Assembly Performance for ...

Not able to train to SuperSpeed – instead, the system is trained to operate at USB 20 high speed Radio frequency interference (RFI) – the proximity of USB 30 connector and cable assembly makes a wireless device, for example a wireless mouse, cease to work Unable to function at all

2-Port USB 3.0 Hub Reference Design

The USB 30 Hub Design is a two-port USB 30 compliant hub It provides simultaneous SuperSpeed and high-speed/full-speed connections on the upstream port and provides SuperSpeed, high-speed, full-speed, or low-speed connections on the downstream ports The hub design provides power control for each downstream port and overcurrent protection

AN 26.2 - Implementation Guidelines for SMSC's USB 2.0 and ...

Implementation Guidelines for SMSC’s USB 20 and USB 30 Hub Devices SMSC AN 262 3 Revision 20 (07-17-13) APPLICATION NOTE Figure 22 Example Switching Regulator Noise Filter 23 VBUS_DET VBUS_DET is used to initiate a connect event to the hub device For stand-alone applications, this should be connected to the upstream VBUS through a resistor

USB Hardware Design Guide - Silicon Labs

USB Hardware Design Guide AN0046 - Application Note A typical example for this would be a smartphone or a tablet that can both connect to a computer as a USB Mass Storage Device, or act as a host if a memory card reader or a USB memory stick is a USB device can either be powered over the USB cable, or it can be self powered The following

CYPRESS SEMICONDUCTOR CORPORATION Internal ...

Does Cypress provide hardware design guidelines for customers building PCBs with FX3? A: Yes, Cypress provides hardware design guidelines for FX3 as part of the AN70707 – EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist application note Q32 Where can I get information about “SuperSpeed Device Design By Example,” by

TUSB73x0 Board Design and Layout Guidelines (Rev. E)

TUSB73x0 Board Design and Layout Guidelines Preface SLLU149E–June 2011–Revised February 2016 TUSB73x0 Board Design and Layout Guidelines These guidelines are intended to provide developers with the resources needed to properly layout the TUSB7320/TUSB7340 They are

intended as a follow-on document to the USB 20 Board Design and

EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic ...

EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist wwwcypresscom Document Number 001-70707 Rev*O 4 3 Power System 31 Overview The EZ-USB FX3 device power domains are shown in Figure 1 A description and the voltage settings on each of these domains are provided in Table 2 Figure 01 EZ-USB FX3 Power Domains Diagram B301x D

Integrating DesignWare USB3.0 Device Controller In a UVM ...

The Synopsys DesignWare Cores SuperSpeed USB30 Controller has four configurations: USB30 Device Controller, USB30 Host Controller, USB30 Static Dual-Role Device Controller systems may use a RTL design or a different vendor’s verification IP as the Host side On the Device side of the example environment, the following setups are made:

Designing with the EZ-USB FX3 Slave FIFO Interface

Designing with the EZ-USB FX3 Slave FIFO Interface wwwcypresscom Document No 001-65974 Rev *O 3 21 EZ-USB FX3 Software Development Kit Cypress delivers the complete software and firmware stack for FX3 to easily integrate SuperSpeed USB into any

How to Prepare for a Design Review - EDGE

How to Prepare for a Design Review Rick Lux MSD I October 2, 2009 Design Reviews • Objectives • Participants • Logistics – Materials for review Example from Low Energy Printing Project P09505 January 16, 2009 Senior Design I - System Level Design Review Project Scope

Optimizing USB 3.0 Throughput With EZ-USB® FX3™

Optimizing USB 30 Throughput With EZ-USB® FX3™ wwwcypresscom Document No 001-86947 Rev *D 2 2 Related Resources Cypress provides a wealth of data at wwwcypresscom to help you select the right device for your design and quickly

CYUSB303X, EZ-USB® FX3S SuperSpeed USB Controller

EZ-USB® FX3S SuperSpeed USB Controller Cypress provides a wealth of data at wwwcypresscom to help you to select the right <product> device for your design, and to help you to quickly and effectively integrate the device into your design Example on Linux